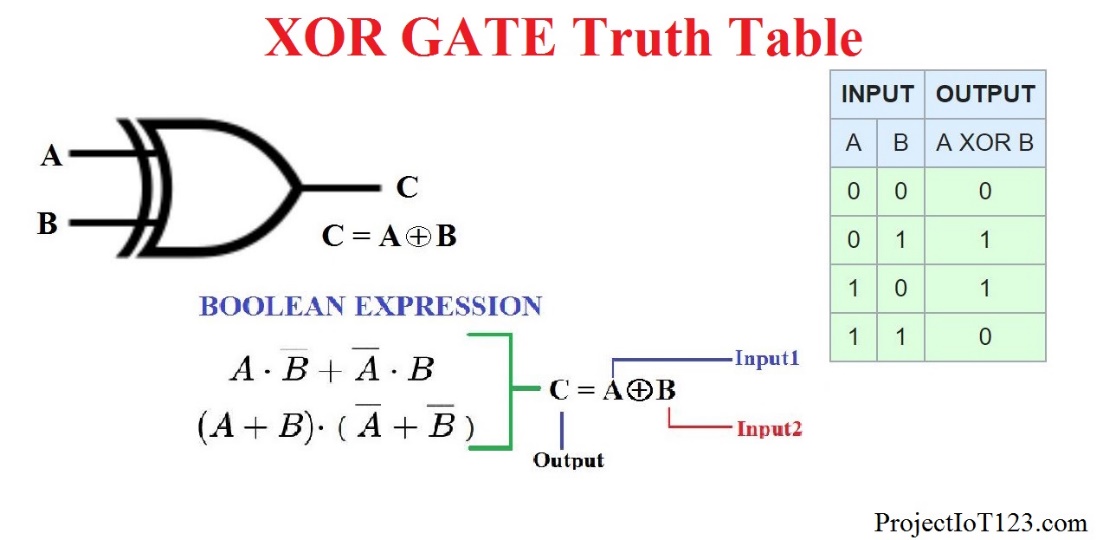
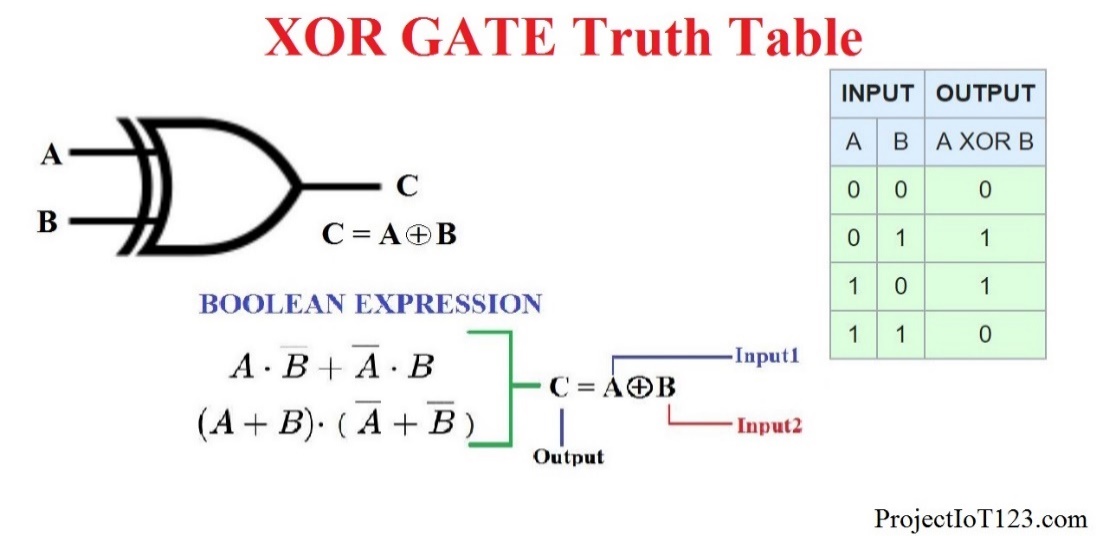
**Circuit Diagram & Truth Table:**

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**Code:**

* **Design Module**

module gate(c,a,b);

inputa,b;

output c;

xor a1(c,a,b);

endmodule

* **TestBench**

Module tb;

rega,b;

wire c;

gate g1(c,a,b);

initial

begin

a=1'b0;b=1'b0;

#20

a=1'b0;b=1'b1;

#20

a=1'b1;b=1'b0;

#20

a=1'b1;b=1'b1;

#20

$finish;

end

endmodule